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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,744	12/26/2001	Motoshige Kobayashi	217760US2S	1638

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,744	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,985,708 Nakagawa et al.

1. Referring to claim 1, a semiconductor device comprising: a first conductivity type base layer, (Figure 12 #44); a second conductivity type base layer, (Figure 12 #51), selectively formed on an upper surface of said first conductivity type base layer, (Figure 12 #44); a first conductivity type emitter layer, (Figure 12 #60), selectively formed on a surface said second conductivity type base layer, (Figure 12 #51); gate electrode, (Figure 12 #57), formed on a part of said second conductivity type base layer, (Figure 12 #51), sandwiched between said first conductivity type emitter layer, (Figure 12 #60), and said first conductivity type base layer, (Figure 12 #44), with a gate insulating film, (Figure 12 #56), interposed between said second conductivity type base layer, (Figure 12 #51), and said gate electrode, (Figure 12 #57); a first conductivity type buffer layer, (Figure 12 #46), formed on a back surface of said first conductivity type base layer, (Figure 12 #44); and a second conductivity type collector layer, (Figure 12 #47), formed on a back surface of said first conductivity type buffer layer, (Figure 12

#46), wherein requirement of d2/dl > 1.5 is satisfied where dl a depth in said first conductivity type buffer layer, (Figure 12 #46), as measured from an interface of said first conductivity type buffer, (Figure 12 #46), layer and said second conductivity type collector layer, (Figure 12 #47), which concentration of a first conductivity type activated impurity in said first conductivity type buffer layer, (Figure 12 #46), shows a peak value and a d2 shallowest depth in said first conductivity type buffer layer, as measured from the interface of said first conductivity type buffer layer, (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #47), at which an activation ratio of said first conductivity type impurity in said first conductivity type buffer layer, (Figure 12 #47), a predetermined value .

* Nakagawa et al. discloses the claimed invention except for the impurity concentration is measured from d2/d1, d1 is the first type impurity concentration depth measured from the first concentration type buffer layer to the second conductivity collector layer, and d2 is the shallowest depth in said first conductivity type buffer layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the impurity concentration relations ship between the buffer and collector layers to be d2/d1 since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

** Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

2. Referring to claim 2, a semiconductor device, wherein said activation ratio is defined by concentration activated those of said first conductivity type impurity in said first conductivity type buffer layer, (Figure 12 #46), /a concentration of said first conductivity type impurity in said first conductivity type buffer layer, (Figure 12 #46).

3. Referring to claim 3, a semiconductor device wherein said concentration of said activated first conductivity type impurity in said conductivity type impurity type buffer layer, (Figure 12 #46), is observed by a Spreading Resistance analysis and said concentration of said first conductivity type impurity in said first conductivity type buffer layer, (Figure 12 #46), is observed by Secondary Ion Mass Spectrometry analysis.

*** Initially, and with respect to claims 3, 5-12, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

4. Referring to claim 4, a semiconductor device, wherein said predetermined value for said activation ratio is substantially 0.3 or lower than 0.3, (See ** above).

5. Referring to claim 5, a semiconductor device, wherein said first conductivity type buffer layer, (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #47), are formed from impurity diffusion layers, (Col. 17 Lines 1-14 & see *** below).

6. Referring to claim 6, a semiconductor device, wherein said first conductivity type buffer layer, (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #47), are formed from impurity diffusion layers, (Col. 17 Lines 1-14 & see *** above).

7. The semiconductor device according claim wherein said first conductivity type buffer layer, (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #47), are formed by implanting impurities into and annealing, (See *** above), a first conductivity type semiconductor wafer, (Figure 12 #46 and 47), having substantially uniform impurity concentration.

8. Referring to claim 8, a semiconductor device, wherein said first conductivity type buffer layer , (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #46), are formed by implanting impurities into and annealing, (See *** above), first conductivity type semiconductor wafer, (Figure 12 #46 and 47), having substantially uniform impurity concentration.

9. Referring to claim 9, a semiconductor device, wherein said first conductivity type base layer, (Figure 12 #44), said second conductivity type base layer, (Figure 12 #51), said first conductivity type emitter layer, (Figure 12 #60), said first conductivity type buffer layer, (Figure 12 #44), and said second conductivity type collector layer, (Figure 12 #47), are formed from impurity diffusion layers, (Col. 17 Lines 1-14 & see *** above).

10. Referring to claim 10, a semiconductor device, wherein said first conductivity type base layer, (Figure 12 #44), said second conductivity type base layer, (Figure 12 #51), said first conductivity type emitter layer, (Figure 12 #60), said first conductivity type buffer layer, (Figure

12 #44), and said second conductivity type collector layer, (Figure 12 #47), are formed from impurity diffusion layers, (Col. 17 Lines 1-14 & see *** above).

11. Referring to claim 11, a semiconductor device, wherein said first conductivity type base layer, (Figure 12 #44), said second conductivity type base layer, (Figure 12 #51), and said first conductivity type emitter layer, (Figure 12 #60), are formed by implanting impurities into a first conductivity type semiconductor wafer having a substantially uniform impurity concentration, and said first conductivity type buffer layer, (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #47), are formed by implanting impurities into and annealing said semiconductor wafer, (See *** above).

13. Referring to claim 12, a semiconductor device, wherein said first conductivity type base layer, (Figure 12 #44), said second conductivity type base layer, (Figure 12 #51), and said first conductivity type emitter layer, (Figure 12 #60), are formed by implanting impurities into a first conductivity type semiconductor wafer having a substantially uniform impurity concentration, and said first conductivity type buffer layer, (Figure 12 #46), and said second conductivity type collector layer, (Figure 12 #47), are formed by implanting impurities into and annealing said semiconductor wafer, (See *** above).

13. Referring to claim 13, a semiconductor device, wherein said depth d2 is larger than said depth dl, (See * and ** above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

VAMJ
August 14, 2003